PHY-439 Electronics-II

Credit Hours: 2-1

Prerequisite: None

Course Description:

Digital Logic Design is a one-semester course taken by Electrical Engineering students during the second year of their engineering program. This course introduces the logic operators and gates to lay the framework for strengthening the basic understanding of computer building blocks. Both combinational and sequential circuits are studied in this course along with their constituent elements comprising Arithmetic circuits, Comparators, Decoders, Encoders, and Multiplexers, Tristate gates as well as Latches, Flip-flops, Counters and Registers. It lays down foundations for advanced studies in Microprocessor Systems to be taught in the following semester.

Detailed Course Contents:

Introduction to digital systems, Number systems, Binary, Octal, decimal and hexadecimal numbers, base conversions, complements and unsigned numbers, signed binary numbers, addition and subtraction, binary codes, binary storage and registers, binary logic and logic gates, Boolean Algebra, Axiomatic definition of Boolean Algebra, basic properties and therems of Boolean Algebra, Canonical and standard forms, Digital logic gates and Integrated circuits, The K-Map method, Sum-of-Products and Products-of-Sums, Quine-McCluskey Minimization algorithm (Tabulation), NAND and NOR implementations, Combinational Circuits their Analysis and design procedure, Decimal Adder, Binary Multiplier, Magnitude Comparator, Decoders, encoders and multiplexers, Sequential Circuits and different types of Latches and Flip-Flops, Analysis of Clocked-Sequential Circuits; State Equations, State Table, State Diagram, and Flip-Flop input equations, Analysis with D Flip-Flops, JK Flip-Flops, and T Flip-Flops. Mealy and Moore Models and conversion procedure, state reduction and assignments, registers and counters.

Text Book:

Digital Design with an Introduction to the Verilog HDL, VHDL, and SystemVerilog (Sixth edition) by M. Morris Mano and Michael Ciletti (MC)

Reference Books:

1. Digital Fundamentals (Eleventh Edition) by Floyd
2. Fundamentals of Logic Design (Sixth Edition)by Charles H. Roth Jr
3. Contemporary Logic Design (Second Edition) by Randy H. Katz

Week	Section	Topics
1.	1.1-1.5 (MC)	Introduction to Digital Systems, Number Systems: Binary, Octal, Decimal and Hexadecimal Numbers and Base Conversions, Complements: Subtraction of Unsigned Numbers using Complements.
2.	1.6-1.9 (MC)	Signed Binary Numbers Arithmetic: Addition and Subtraction of Signed Binary Numbers. Binary Codes. Binary Storage and Registers. Binary Logic: Definition of Binary Logic and Logic gates.
3.	2.1-2.6 (MC)	Boolean Algebra: Basic and Axiomatic Definition of Boolean Algebra; Two-Valued Boolean Algebra. Basic Theorems and Properties of Boolean Algebra. Boolean Functions; Canonical and Standard Forms.
4.	2.7-2.9 (MC)	Other Logic Operations. Digital Logic Gates and Integrated Circuits.
5.	3.1-3.3 (MC)	The K-Map Method; Two, Three, Four, and Five -Variable K-Maps. Sum-of-Products (SOP) simplification using map method. Essential and Non- essential Prime Implicants.
6.	3.4-3.6 (MC) + Handouts	Product- of- Sums (POS) Simplifications and Don't Care conditions. Quine-McCluskey Minimization algorithm (Tabulation). NAND and NOR implementations.
7.	3.7-3.8 (MC) + Handouts	Other Two-Level implementations. Exclusive-OR function: Parity Generation and Checking.
8.	4.1-4.5	Combinational Circuits and Analysis and design Procedure.

	(MC)	Design of 4-bit Ripple Carry and Carry Look-ahead Adder-Subtractor using Full Adders
	Midterm	
9.	4.6-4.9 (MC)	Decimal Adder. Binary Multiplier. Magnitude Comparator. Decoders/De-multiplexers.
10.	4.10-4.11 (MC)	Encoders. Multiplexers and Tri-State Gates.
11.	5.1-5.4 (MC)	Sequential Circuits and different types of Latches and Flip-Flops.
12.	5.5 (MC)	Analysis of Clocked-Sequential Circuits; State Equations, State Table, State Diagram, and Flip-Flop input equations. Analysis with D Flip-Flops, JK Flip-Flops, and T Flip-Flops. Mealy and Moore Models and Conversion Procedure.
13.	5.7, 5.8 (MC)	State Reduction using Row Matching and Implication Table Techniques. State Assignment Method. Design Procedure-Synthesis using D, JK, and T Flip-Flops.
14.	6.1-6.2 (MC)	Registers with Parallel Load. Shift Registers; 4-Bit Shift Register; Serial Transfer and Serial Addition. 4-Bit Universal Shift Register.
15.	6.3-6.5 (MC)	Ripple Counters; Binary and BCD Ripple Counters. Synchronous Counters; Binary and BCD Counters.
16.		Revision
17.	**End Semester Exam**	